What is claimed is:

1. A semiconductor integrated circuit having over one semiconductor substrate a nonvolatile memory and a logic circuit which uses information stored in said nonvolatile memory to perform logical operation,

wherein said nonvolatile memory comprises bit lines, word lines, and memory cells,

wherein said memory cell comprises a MOS transistor whose gate electrode is connected with a word line, and information storage is carried out according to whether one source/drain electrode of said MOS transistor is connected with a current path or floated, and

wherein a control circuit is provided which produces a potential difference between the source/drain electrodes of said MOS transistor during a predetermined period in the operation of accessing said memory cell, and makes zero the potential difference between the source/drain electrodes of said MOS transistor during the other periods than said predetermined period.

2. The semiconductor integrated circuit according to Claim 1,

wherein the time at which a potential difference is produced between the source/drain electrodes of said

MOS transistor is matched with or behind the time at which a word line is selected.

3. The semiconductor integrated circuit according to Claim 1,

wherein said nonvolatile memory and logic circuit use common supply voltage as their operating power supply voltage.

4. The semiconductor integrated circuit according to Claim 1,

wherein whether a MOS transistor is connected with said current path or floated is determined according to whether the one source/drain electrode thereof on the opposite side to the bit line is connected with a predetermined signal line or not.

5. The semiconductor integrated circuit according to Claim 1 or Claim 4,

wherein the MOS transistors respectively included in a plurality of memory cells disposed along said bit lines are formed in a common well, and are electrically separated from each other by a dummy MOS transistor whose gate electrode is supplied with off potential.

6. The semiconductor integrated circuit according

to Claim 4,

wherein one memory cell has two MOS transistors, and the other source/drain electrodes of the two MOS transistors are connected with separate bit lines which constitute complementary bit lines and the gate electrodes of the two MOS transistors are connected with a common word line.

7. The semiconductor integrated circuit according to Claim 5,

wherein one memory cell has two MOS transistors, and the other source/drain electrodes of the two MOS transistors are connected with separate bit lines which constitute complementary bit lines and the gate electrodes of the two MOS transistors are connected with a common word line.

8. The semiconductor integrated circuit according to Claim 6, further comprising an amplifier which amplifies the potential difference between said complementary bit lines.

9. The semiconductor integrated circuit according to Claim 7, further comprising an amplifier which amplifies the potential difference between said complementary bit lines.

10. A semiconductor integrated circuit having over one semiconductor substrate a nonvolatile memory and a logic circuit which uses information stored in said nonvolatile memory to perform logical operation,

wherein said nonvolatile memory comprises memory cells, word lines, complementary bit lines, and differential amplifiers connected with said complementary bit lines, and

wherein said memory cell comprises a pair of MOS transistors whose gate electrodes are connected with the same word line, one source/drain electrodes of the MOS transistors are separately connected with a corresponding bit line of the complementary bit lines, the other source/drain electrode of one MOS transistor is connected with a voltage signal line supplied with predetermined voltage, and the other source/drain electrode of the other MOS transistor is floated.

11. The semiconductor integrated circuit according to Claim 10,

wherein said nonvolatile memory and logic circuit use common supply voltage as their operating power supply voltage.

12. A semiconductor integrated circuit having over

one semiconductor substrate a nonvolatile memory and a logic circuit which uses information stored in said nonvolatile memory to perform logical operation,

wherein said nonvolatile memory comprises memory cells, word lines, complementary bit lines, and differential amplifiers connected with said complementary bit lines,

wherein said memory cell comprises a pair of MOS transistors whose gate electrodes are connected with the same word line; the source/drain electrodes of one MOS transistor are connected with a bit line and a voltage signal line supplied with predetermined voltage, and the source/drain electrodes of the other MOS transistor are floated with respect to a bit line or said voltage signal line, and

wherein during a predetermined period in the operation of accessing said memory cell, voltage is applied to said voltage signal line which voltage produces a potential difference between the voltage signal line and said bit line, and during the other periods than said predetermined period, voltage is applied which makes zero the potential difference between the voltage signal line and said bit line.

13. The semiconductor integrated circuit according to Claim 12,

wherein said nonvolatile memory and logic circuit use common supply voltage as their operating power supply voltage.

14. The semiconductor integrated circuit according to Claim 12,

wherein during the other periods than said predetermined period in accessing operation, said voltage signal lines and complementary bit lines are brought to supply voltage, and during said predetermined period, said voltage signal lines are discharged to the ground voltage of the circuit.

15. The semiconductor integrated circuit according to Claim 14,

wherein the time at which said voltage signal lines are discharged to the ground voltage of the circuit during said predetermined period is matched with or behind the time at which a memory cell is selected by word line.

16. A semiconductor integrated circuit having over one semiconductor substrate a nonvolatile memory and a logic circuit which uses information stored in said nonvolatile memory to perform logical operation,

wherein said nonvolatile memory and logic circuit

use common supply voltage as their operating power supply voltage,

wherein said nonvolatile memory comprises memory cells, word lines, complementary bit lines, and differential amplifiers connected with said complementary bit lines,

wherein said memory cell comprises a pair of MOS transistors whose gate electrodes are connected with the same word line, the source/drain electrodes of one MOS transistor are connected with a bit line and a voltage signal line supplied with predetermined voltage, and the source/drain electrodes of the other MOS transistor are floated with respect to a bit line or said voltage signal line, and

wherein said MOS transistors respectively included in a plurality of memory cells disposed along said bit lines are formed in a common well, and the MOS transistors are electrically separated from each other by a dummy MOS transistor whose gate electrode is supplied with off potential.

17. A semiconductor integrated circuit having over one semiconductor substrate a nonvolatile memory and a logic circuit which uses information stored in said nonvolatile memory to perform logical operation,

wherein said nonvolatile memory and logic circuit

use common supply voltage as their operating power supply voltage,

wherein said nonvolatile memory comprises bit lines, word lines, and memory cells,

wherein said memory cell comprises a MOS transistor whose gate electrode is connected with a word line, and information storage is carried out according to whether one source/drain electrode of said MOS transistor is connected with a current path or floated,

wherein whether a MOS transistor is connected with said current path or floated is determined according to whether the one source/drain electrode thereof on the opposite side to the bit line is connected with a predetermined signal line or not, and

wherein the MOS transistors respectively included in a plurality of memory cells disposed along said bit lines are formed in a common well, and are electrically separated from each other by a dummy MOS transistor whose gate electrode is supplied with off potential.

18. A semiconductor integrated circuit having a nonvolatile memory,

wherein said nonvolatile memory comprises complementary bit lines, word lines, memory cells connected with said complementary bit lines and said word lines, and differential amplifiers connected with

said complementary bit lines,

wherein said memory cell comprises a first MOS transistor having one source/drain electrode connected with one bit line of said complementary bit lines and a gate electrode connected with said word line, and a second MOS transistor having one source/drain electrode connected with the other bit line of said complementary bit lines and a gate electrode connected with said word line,

wherein the other source/drain electrode of said first MOS transistor is connected with a voltage signal line supplied with predetermined voltage, and

wherein the other source/drain electrode of said second MOS transistor is floated.

19. A semiconductor integrated circuit having a nonvolatile memory,

wherein said nonvolatile memory comprises complementary bit lines, word lines, memory cells connected with said complementary bit lines and said word lines, and differential amplifiers connected with said complementary bit lines,

wherein said memory cell comprises a first MOS transistor having one source/drain electrode connected with one bit line of said complementary bit lines and a gate electrode connected with said word line, and a

second MOS transistor having one source/drain electrode connected with the other bit line of said complementary bit lines and a gate electrode connected with said word line,

wherein the other source/drain electrode of said first MOS transistor is connected with a voltage signal line supplied with predetermined voltage, and

wherein during the other periods than a predetermined period in the operation of accessing the memory cell, voltage which makes zero the potential difference between the voltage signal line and the one source/drain electrode is applied to said voltage signal line.

20. The semiconductor integrated circuit according to Claim 19,

wherein during the periods other than a predetermined period in the operation of accessing said memory cell, said voltage signal lines and bit lines are brought to supply voltage.

21. The semiconductor integrated circuit according to Claim 19,

wherein during a predetermined period in the operation of accessing said memory cell, said voltage signal lines are discharged to the ground voltage of

the circuit.

22. The semiconductor integrated circuit according to Claim 21,

wherein the time at which said voltage signal lines are discharged to the ground voltage of the circuit during said predetermined period is matched with or behind the time at which a memory cell is selected by word line.

23. A semiconductor integrated circuit having a nonvolatile memory,

wherein said nonvolatile memory comprises complementary bit lines, word lines, memory cells connected with said complementary bit lines and said word lines, and differential amplifiers connected with said complementary bit lines,

wherein said memory cell comprises a first MOS transistor having one source/drain electrode connected with one bit line of said complementary bit lines and a gate electrode connected with said word line, and a second MOS transistor having one source/drain electrode connected with the other
bit line of said complementary bit lines and a gate electrode connected with said word line,

wherein in each memory cell, the other source/drain

electrode of either said first MOS transistor or second MOS transistor is connected with a voltage signal line supplied with predetermined voltage, and

wherein a third transistor is formed between the other source/drain electrodes of the first MOS transistors which adjoin to each other and share a bit line between them, and the third transistor is controlled to off state.

24. A semiconductor integrated circuit having a nonvolatile memory,

wherein said nonvolatile memory comprises complementary bit lines, first word lines, second word lines, first memory cells connected with said complementary bit lines and said first word lines, second memory cells connected with said complementary bit lines and said second word lines, and differential amplifiers connected with said complementary bit lines,

wherein said first memory cell comprises a first MOS transistor having a source-drain path connected between a voltage signal line supplied with predetermined voltage and one bit line of said complementary bit lines, and a gate electrode connected with said first word line, and a second MOS transistor having source/drain electrodes any one of which is floated and a gate electrode connected with said first

word line,

wherein said second memory cell comprises a third MOS transistor having a source-drain path connected between said voltage signal line and said one bit line of said complementary bit lines, and a gate electrode connected with said second word line, and a fourth MOS transistor having source/drain electrodes any one of which is floated and a gate electrode connected with said second word line,

wherein a fifth transistor is provided which has source/drain electrodes connected with one of the source/drain electrodes of said first MOS transistor and one of the source/drain electrodes of said third MOS transistor, and is controlled to off state, and

wherein a sixth transistor is provided which has source/drain electrodes connected with one of the source/drain electrodes of said second MOS transistor and one of the source/drain electrodes of said fourth MOS transistor, and is controlled to off state.

25. The semiconductor integrated circuit according to Claim 24,

wherein the other of said source/drain electrodes of said second MOS transistor is connected with the other of said complementary bit lines, and

wherein the other of said source/drain electrodes

of said fourth MOS transistor is connected with the other of said complementary bit lines.

26. The semiconductor integrated circuit according to Claim 25,

wherein during the other periods than a predetermined period in the operation of accessing said nonvolatile memory, voltage which substantially makes zero the potential difference between the source/drain electrodes of said first and third MOS transistors is applied to said voltage signal line.

27. The semiconductor integrated circuit according to Claim 25,

wherein a circuit is provided which substantially makes zero the potential difference between the source/drain electrodes of said first MOS transistor and the potential difference between the source/drain electrodes of said third MOS transistor during a first period in the operation of accessing said nonvolatile memory, and produces a predetermined potential difference between the source/drain electrodes of said first MOS transistor and between the source/drain electrodes of said third MOS transistor during a second period in the operation of accessing said nonvolatile memory.

28. The semiconductor integrated circuit according to Claim 24,

wherein a circuit is provided which substantially makes zero the potential difference between the source/drain electrodes of said first MOS transistor and the potential difference between the source/drain electrodes of said third MOS transistor during a first period in the operation of accessing said nonvolatile memory, and produces a potential difference between the source/drain electrodes of said first MOS transistor and between the source/drain electrodes of said third MOS transistor during a second period in the operation of accessing said nonvolatile memory.

29. A semiconductor integrated circuit having a nonvolatile memory,

wherein said nonvolatile memory comprises bit lines, first word lines, second word lines, first memory cells connected with said bit lines and said first word lines, second memory cells connected with said bit lines and said second word lines, and amplifiers connected with said bit lines,

wherein said first memory cell comprises a first MOS transistor having source/drain electrodes connected with a voltage signal line supplied with

predetermined voltage and said bit line, and a gate electrode connected with said first word line,

wherein said second memory cell comprises a second MOS transistor having source/drain electrodes one of which is floated and the other of which is connected with said bit line, and a gate electrode connected with said second word line, and

wherein a circuit is provided which substantially makes zero the potential difference between the source/drain electrodes of said first MOS transistor during a first period in the operation of accessing said nonvolatile memory, and produces a predetermined potential difference between the source/drain electrodes of said first MOS transistor during a second period in the operation of accessing said nonvolatile memory.

30. The semiconductor integrated circuit according to Claim 29,

wherein a third transistor is provided which has source/drain electrodes connected with one of the source/drain electrodes of said first MOS transistor and one of the source/drain electrodes of said second MOS transistor, and is controlled to off state.

31. A semiconductor integrated circuit having a

nonvolatile memory,

wherein said nonvolatile memory comprises bit lines, first word lines, second word lines, first memory cells connected with said bit lines and said first word lines, second memory cells connected with said bit lines and said second word lines, and amplifiers connected with said bit lines,

wherein said first memory cell comprises a first MOS transistor having source/drain electrodes connected with a voltage signal line supplied with predetermined voltage and said bit line, and a gate electrode connected with said first word line,

said second memory cell comprises a second MOS transistor having source/drain electrodes one of which is floated and the other of which is connected with said bit line, and a gate electrode connected with said second word line, and

wherein a third transistor is provided which has source/drain electrodes connected with one of the source/drain electrodes of said first MOS transistor and the other of the source/drain electrodes of said second MOS transistor, and is controlled to off state.